I CLAIM:

1. A packaged semiconductor device, comprising:
   a substrate, said substrate comprising:
      a patterned metal layer having first and second surfaces and openings extending between said first and second surfaces;
      a first insulating layer covering said first surface and extending into said openings such that said first insulating layer in said openings is coplanar with said second surface;
      a second insulating layer covering a portion of said second surface of said patterned metal layer and said openings;
   an integrated circuit chip having active and passive surfaces, said passive surface attached to said first insulating layer; and
   plastic encapsulation material covering said chip.

2. The device according to Claim 1, wherein said second insulating layer is solder resist.

3. The device according to Claim 1, wherein said second insulating layer has a thickness less than about 30 μm.

4. The device according to Claim 1, wherein said metal layer comprises copper and has a thickness in the range of 10 to 35 μm.

5. A substrate for a semiconductor package, comprising:
   a sheet-like plastic carrier having first and second surfaces;
   a patterned metal layer removably attached to said first surface of said plastic carrier; and
   an insulating layer on said second surface of said plastic carrier.

6. The substrate according to Claim 5, wherein said plastic carrier is a polyimide film having a thickness in the range of about 30 μm to 80 μm.

7. The substrate according to Claim 5, wherein said metal layer comprises copper and has a thickness in the range of 10 to 35 μm.

8. The substrate according to Claim 5, wherein said second insulating layer is solder resist.

9. The substrate according to Claim 5, wherein said second insulating layer has a thickness less than about 30 μm.

10. A method for packaging an integrated circuit chip, said chip including active and passive surfaces with contact pads on said active surface, said method comprising the steps of:

providing a substrate, said substrate comprising:

a carrier tape;

a patterned metal layer having first and second surfaces and openings extending between said first and second surfaces, said second surface of said patterned metal layer removably attached to said carrier tape;

a first insulating layer covering said first surface of said patterned metal layer and portions of said carrier tape exposed in said openings in said patterned metal layer;

attaching said integrated circuit chip to said first insulating layer on said substrate;

encapsulating said chip; and

removing said carrier tape from said patterned metal layer to expose said second surface of said patterned metal layer.

11. The method according to Claim 10, further comprising

the step of:

applying a second insulating layer to said second surface of said patterned metal layer, said second insulating layer covering a portion of said second surface of said patterned metal layer and leaving said second surface of said patterned metal layer exposed in windows in said second insulating layer.

12. The method according to Claim 11, further comprising the step of:

attaching solder balls to said second surface of said patterned metal layer exposed in said windows in said second insulating layer.

13. The method according to Claim 10, wherein said step of removing said carrier tape is preceded by the step of exposing said carrier tape to infrared radiation.

14. The method according to Claim 10, wherein said step of removing said carrier tape is preceded by the step of exposing said carrier tape to ultra-violet radiation.

15. The method according to Claim 11, wherein said step of applying a second insulating layer comprises applying less than 30 μm of insulating layer to said second surface of said patterned metal layer.

16. The method according to Claim 11, wherein said step of applying a second insulating layer comprises applying solder resist to said second surface of said patterned metal layer.

17. The method according to Claim 10, wherein said step of providing a substrate with a first insulating layer comprises providing a substrate with a solder resist layer covering said first surface of said patterned metal layer.